Frequently Asked EMC Questions (and Answers)

Elya B. Joffe
K.T.M. Project Engineering
e-mail: eb.joffe@ieee.org

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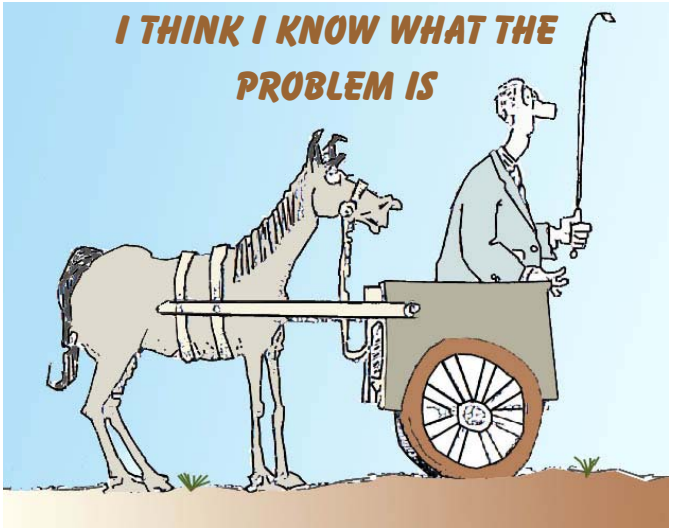
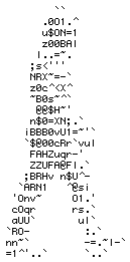


TOP 12 EMC QUESTIONS...

12,...11...10

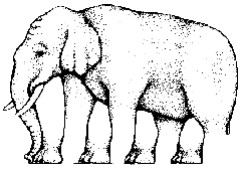


3,...2,...1

12. Is "the larger (decoupling capacitors) the better"?

Correct answer: It depends

- How much charge must you transfer?
- What is the frequency band of concern?
- How much inductance (ESL) can you tolerate



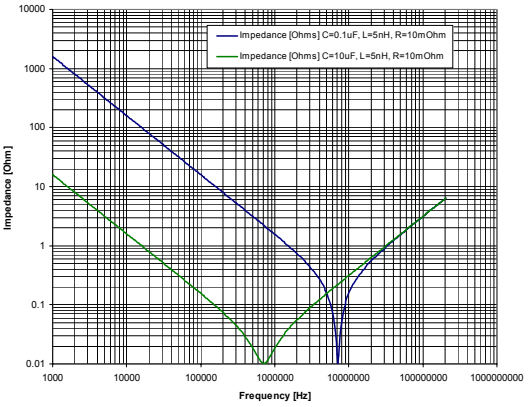
Nothing is like it seems...

Good answer: Yes

Once you have chosen a package size for your capacitor (e.g., 0603, 0402) use the largest capacitance you can "buy"

12. Is "the larger (decoupling capacitors) the better"?

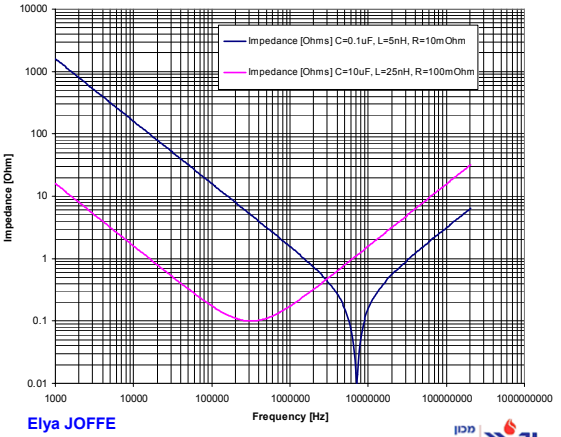
- HF impedance dominated by inductance (ESL), which depends on package size…
- For a given package size, the ESL is "fixed": Capacitance determines resonance and low frequency performance
- Capacitor Installation dominates factor at high frequencies



Chapter Colloquium on Electromagnetic Interference (EMI) in Radio Systems:
Applications in Communication Engineering, Satellite Communications, Electromagnetic Compatibility, Microwave, antennae and Electron Devices

12. Is "the larger (decoupling capacitors) the better?

- HF impedance dominated by inductance (ESL), which depends on package size…
- Capacitor Installation becomes the dominant factor!



11. Are two decoupling capacitors better than one?

Correct answer: It depends

- At reducing power bus noise?
- What is the nominal value?
- How are they connected?
- Is power bus noise even a problem with this design?
- How important is board area? Reliability?

Good answer: Yes.

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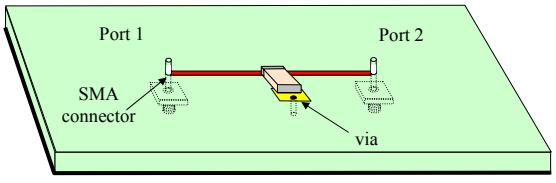
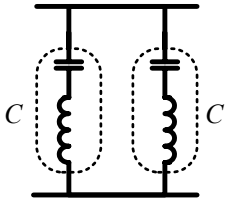
11. Are two decoupling capacitors better than one?



Courtesy: Prof. T. Hubing
University of Missouri-Rolla



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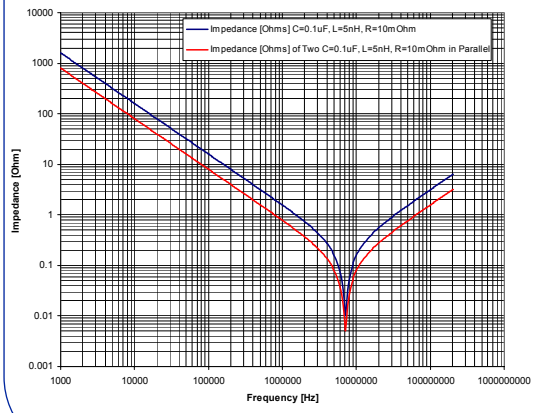
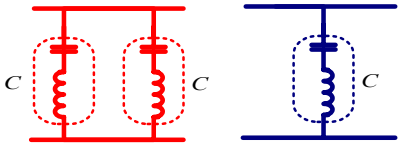


- Impedance goes down
- No change in resonant frequency

$$F_{RES} = \frac{1}{2\pi\sqrt{(L \parallel L)\cdot(C \parallel C)}} \approx$$

$$\approx \frac{1}{2\pi\sqrt{(L/2)\cdot(2C)}} = \frac{1}{2\pi\sqrt{LC}}$$



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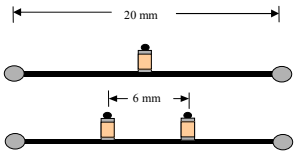

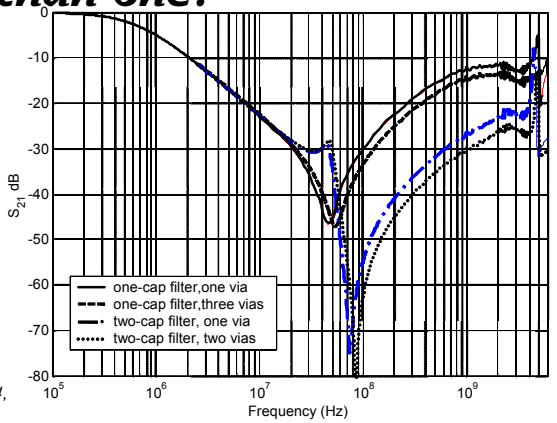

Source: T. Zeeff, T. Hubing, T. Van Doren and D. Pommerenke, "Analysis of simple two-capacitor low-pass filters," IEEE Transactions on Electromagnetic Compatibility, vol. 45, no. 4, Nov. 2003, pp. 595-601.

Courtesy: Prof. T. Hubing
University of Missouri-Rolla

10. Are two unequal decoupling capacitors better than two equal ones?

Correct answer: It depends

- For wideband decoupling?
- For bulk decoupling or IC decoupling?
- Power System Impedance objective?

Good answer: Yes.- for bulk capacitors

No - for IC decoupling

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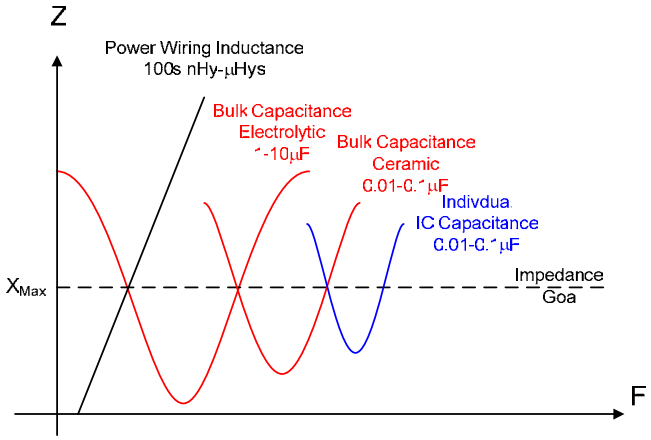

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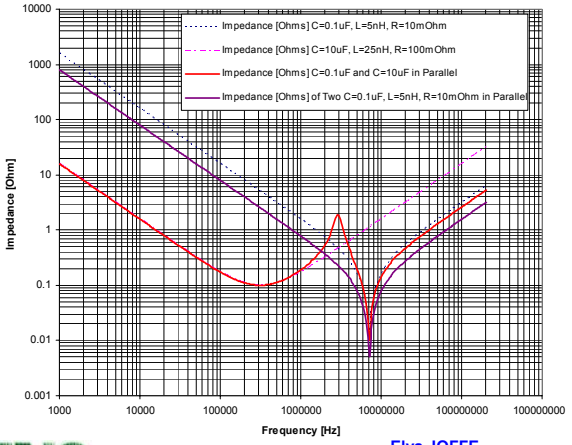

- Equal parallel caps:
  - Lower Impedance
  - Narrow BW
  - Same resonance frequency
- Different parallel caps:
  - Lower LF impedance
  - Broad BW
  - New, Parallel resonance!

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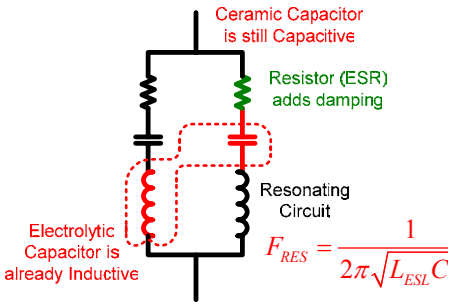

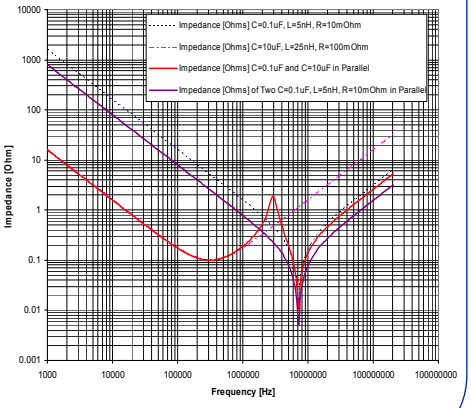

Elya JOFFE
Frequently Asked EMC Questions (and Answers)

9. Should inductors be included in series with the decoupling capacitor?

Correct answer: It depends

- Need filtering?
- In single-layer/multi-layer PCB?
- Why should we?

Good answer: No!

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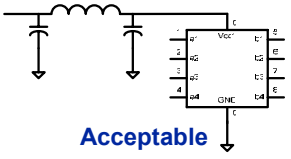
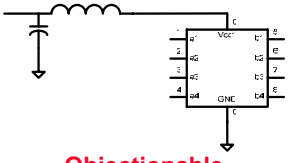
9. Should inductors be included in series with the decoupling capacitor?

- **Power isolation/filtering for sensitive circuits, e.g., analog circuits**
- **Power isolation for clocks and I/O Power**
- **Ferrite beads preferred over inductors**
  - Reduce circuit Q and increase damping
- **Avoid if not in external layer**



Acceptable

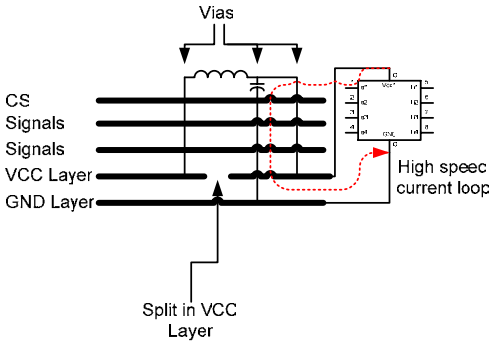
- **In decoupling schemes we try to work against inductance**
- **Choke will also choke the IC**
- **Avoid if not in external layer**



Objectionable
"Chokes" the device

9. Should inductors be included in series with the decoupling capacitor?

- **Four objections:**
  - Normally not necessary
  - Requires splitting of VCC Plane → increasing inductance → problematic in pulsed current
  - Inductor is a current differentiator, not an integrator (LPF) → emphasizes current noise
  - Via inductance
- **Advantage to Ferrite-based filters**
  - R-C filter (lossy)

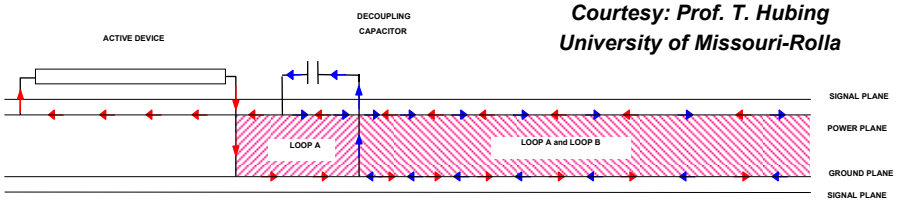


8. Is it better to locate decoupling capacitors near the Vcc pin or near the ground pin of an active device?

Correct answer: It depends

- Single/Multi-layer board?
- PWR/GND Layer allocation
- IC technology?
- Minimum current path inductance?

Courtesy: Prof. T. Hubing
University of Missouri-Rolla



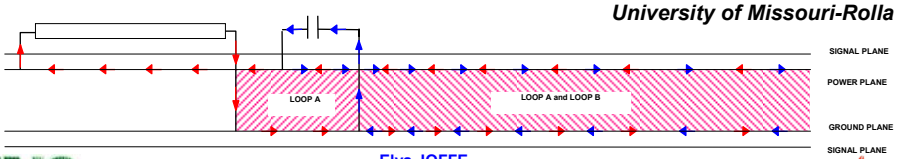
8. Is it better to locate decoupling capacitors near the Vcc pin or near the ground pin of an active device?

Good answer: The name of the game is INDUCTANCE

Inductance of a decoupling capacitor connection is usually more important than the location

However, on boards with a power and ground planes spaced more than 0.5 mm apart, locate the capacitor near the pin connected to the most distant plane.

Courtesy: Prof. T. Hubing
University of Missouri-Rolla



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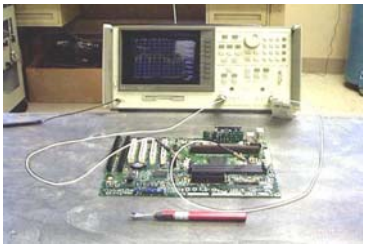
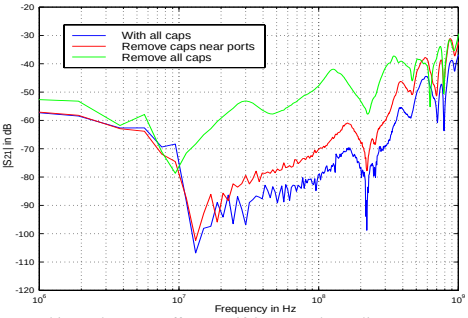




J. Fan, J. Drewniak, J. Knighten, N. Smith, A. Orlandi, T. Van Doren, T. Hubing and R. DuBroff, "Quantifying SMT decoupling capacitor placement in DC power-bus design for multilayer PCBs," *IEEE Transactions on Electromagnetic Compatibility*, vol. 43, no. 4, Nov. 2001, pp. 588-599.

J. Chen, M. Xu, T. Hubing, J. Drewniak, T. Van Doren, and R. DuBroff, "Experimental evaluation of power bus decoupling on a 4-layer printed circuit board," *Proc. of the 2000 IEEE International Symposium on Electromagnetic Compatibility*, Washington D.C., August 2000, pp. 335-338.

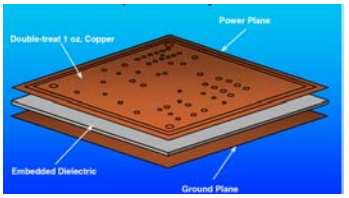
7. How effective is embedded capacitance for reducing EMI?

Correct answer: It depends

- Space constraints on PCBs
- Is cost a factor?

Good answer: If power bus noise was your problem, your problem is solved

Assuming you are using the newer materials with an plane spacing of a few microns and assuming there are no cost, reliability or multiple source issues.

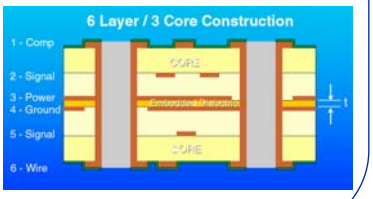


Source: National Center for Manufacturing Sciences "An Overview of the NCMS Embedded Capacitance An Overview of the NCMS Embedded Capacitance Project"

7. How effective is embedded capacitance for reducing EMI?

- **Embedded capacitance makes use of inter-plane capacitance between closely spaced PWR and GND planes**
- **Why Embedded Capacitance?**
  - Increased packaging density
    - Frees up valuable real estate
    - Potential for reducing size and number of layers
  - Lower inductance
    - Improved electrical performance
    - Reduces power bus noise and EMI
  - Quality and Reliability improvement
    - Reduces the number of capacitors
    - Reduces the number of solder joints

Source: National Center for Manufacturing Sciences "An Overview of the NCMS Embedded Capacitance An Overview of the NCMS Embedded Capacitance Project"



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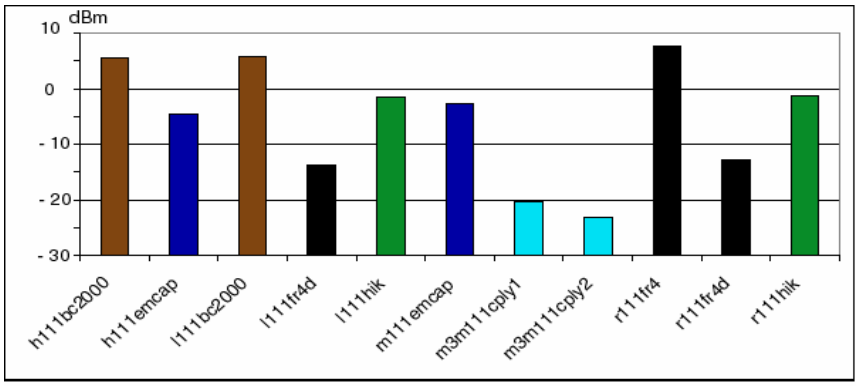


M. Xu, T. Hubing, J. Chen, T. Van Doren, J. Drewniak and R. DuBroff, "Power bus decoupling with embedded capacitance in printed circuit board design," *IEEE Transactions on Electromagnetic Compatibility*, vol. 45, no. 1, Feb. 2003, pp. 22-30.

Courtesy: Prof. T. Hubing
University of Missouri-Rolla

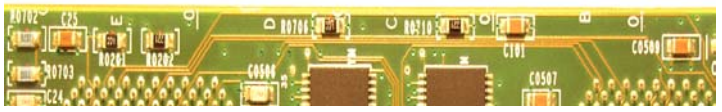
6. Does it matter if traces are routed along the edge of a PCB?

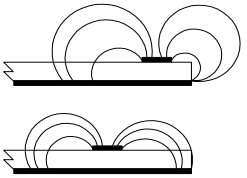
Correct answer: It depends

- For reducing emissions from the PCB?
- For precluding common mode noise emissions?

Courtesy: Prof. T. Hubing
University of Missouri-Rolla

Good answer: Yes. Route high-speed traces at least 10 trace heights away from edge.





Source: Y. Kayano, M. Tanaka, J. Drewniak, and H. Inoue, "Common-Mode Current Due to a Trace near a PCB Edge and its Suppression by a Guard Band," IEEE Transactions on Electromagnetic Compatibility vol. 46, no. 1, Feb. 2004, pp. 46-53.

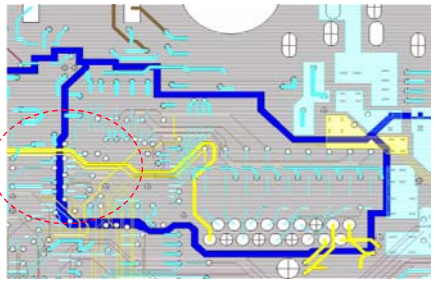
5. If I have to route traces over a gap I the ground plane, what precautions should I take?

Correct answer: It depends

- Layer allocation constraints?

Good answer: Don't do it.

- Rearrange layers
- Change routing



Courtesy: Prof. T. Hubing
University of Missouri-Rolla

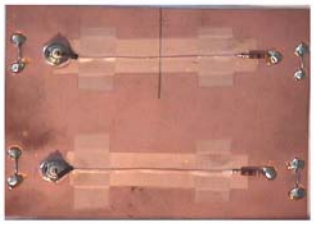
D. M. Hockanson, J. L. Drewniak, T. H. Hubing, T. P. Van Doren, F. Sha, C. W. Lam, and L. Rubin, "Quantifying EMI resulting from finite-impedance reference planes," *IEEE Transactions on Electromagnetic Compatibility*, vol. 39, no. 4, Nov. 1997, pp. 286-297.

T. Zeeff, T. Hubing and T. Van Doren, "Traces coupling across gaps in return planes," accepted for publication in the *IEEE Transactions on Electromagnetic Compatibility*.

5. If I have to route traces over a gap I the ground plane, what precautions should I take?

Practical answer: Be aware of the consequences…

- **1kV ESD injected onto PCB with and without split**
- **Noise coupled into a test circuit was measured**



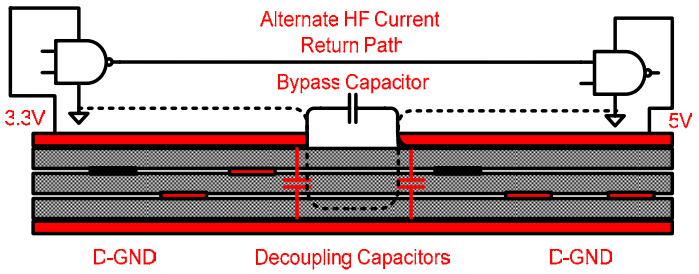
Split Ground Plane Test Board

Overall Test Setup - Front View

Source: "ESD and EMI Effects in Printed Wiring Boards", by Douglas C. Smith

5. If I have to route traces over a gap I the ground plane, what precautions should I take?

Can't bypass caps help out?



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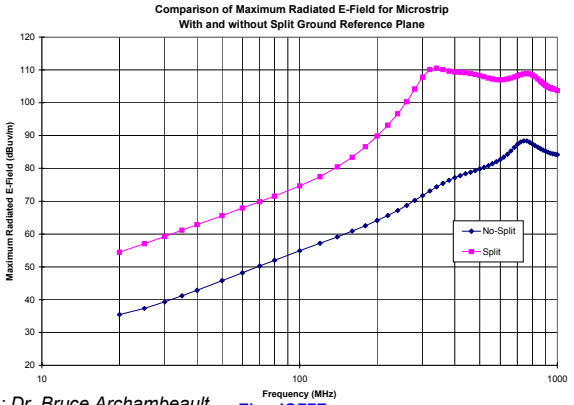

Source: Dr. Bruce Archambeault

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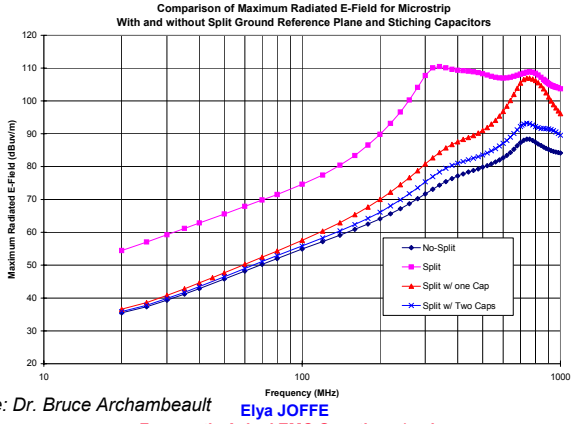

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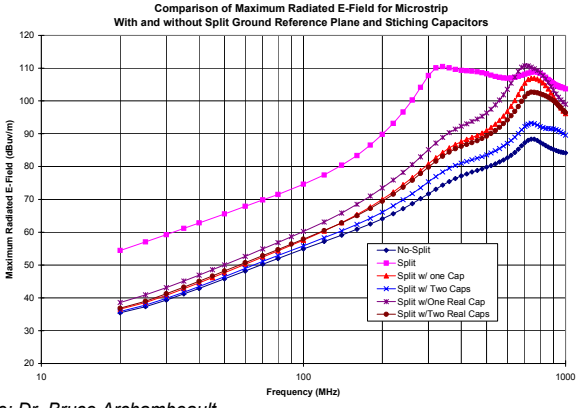
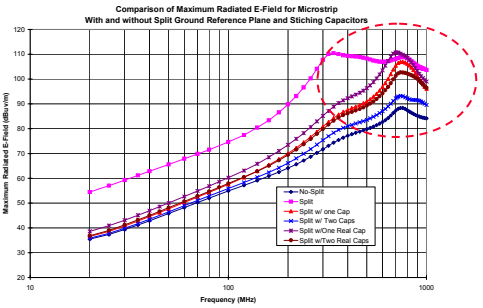


Source: Dr. Bruce Archambeault

5. If I have to route traces over a gap I the ground plane, what precautions should I take?

Can't bypass caps help out?

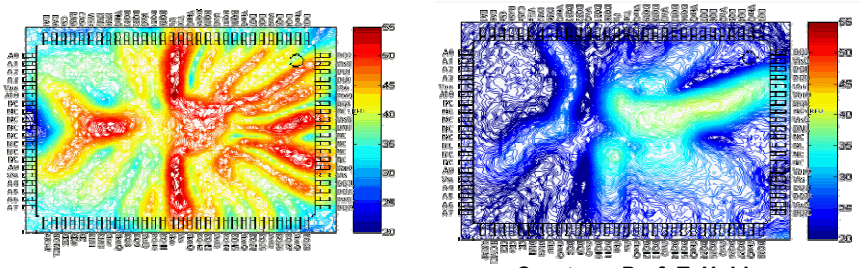
- **YES, at low frequencies**
- **No, at high frequencies**
- ***Need to***
  - *Limit the high frequency current spectrum*
  - *Avoid split crossings with ALL critical signals at the first place*



4. Are VLSI devices important sources of EMI?

Correct answer: It depends

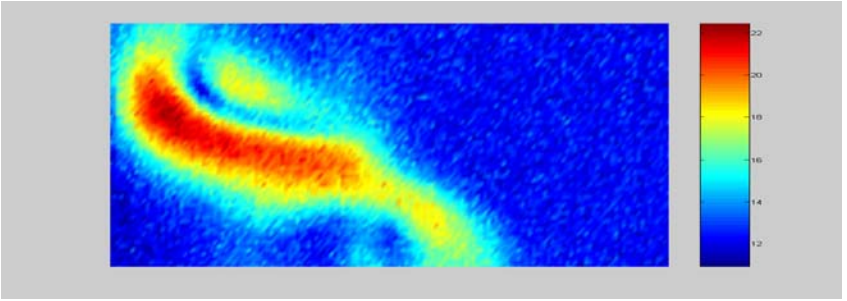
Good answer: Yes. They won't radiated significantly without help from the board, but a poorly designed VLSI device can make the board designer's job extremely difficult.



Courtesy: Prof. T. Hubing
University of Missouri-Rolla

4. Are VLSI devices important sources of EMI?

Differential Clock Driver



T. Hubing, D. Beetner, S. Deng and X. Dong, "Radiation Mechanisms for Semiconductor Devices and Packages," *Proc. of the 2004 International Symposium on Electromagnetic Compatibility - EMC'04 Sendai*, Sendai, Japan, June 2004, 3A1-3.

Courtesy: Prof. T. Hubing
University of Missouri-Rolla

3. How tightly do the lengths of traces in a differential pair need to be controlled to avoid an EMI problem?

Correct answer: It depends

- Transmission line effects (Signal Integrity Concerns)?
- Common mode noise (EMC Concerns)?

Good answer: If it matters at all, then about 0.1 rise time-lengths.

Courtesy: Prof. T. Hubing
University of Missouri-Rolla

T. Hubing, N. Hubing and C. Guo, "Effect of Delay Skew and Transition Time Differences on the Common-Mode Component of Differential Signals," UMR EMC Laboratory Technical Report TR01-8-002, Oct. 1, 2001.

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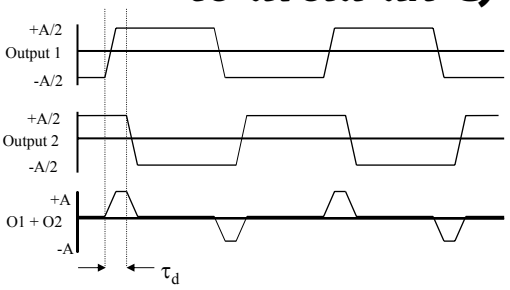
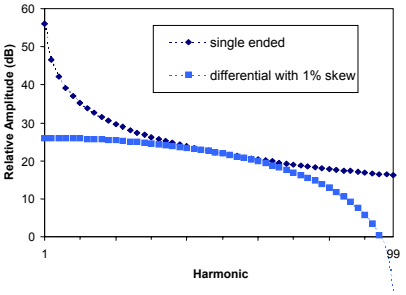


Courtesy: Prof. T. Hubing
University of Missouri-Rolla

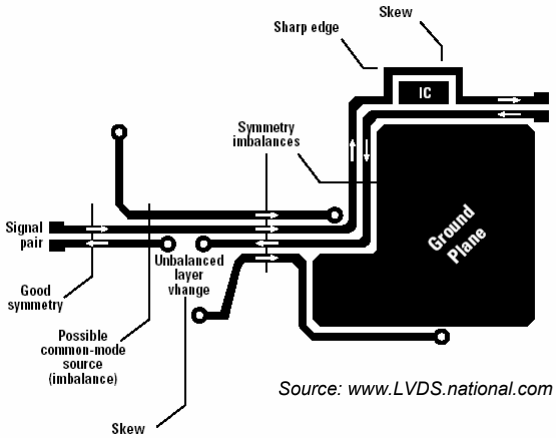


- **Skew is a source of CM noise**
- ***Unequal traces with create imbalance on the transmission lines***
  - *Critical for LVDS*

T. Hubing, N. Hubing and C. Guo, "Effect of Delay Skew and Transition Time Differences on the Common-Mode Component of Differential Signals," UMR EMC Laboratory Technical Report TR01-8-002, Oct. 1, 2001.

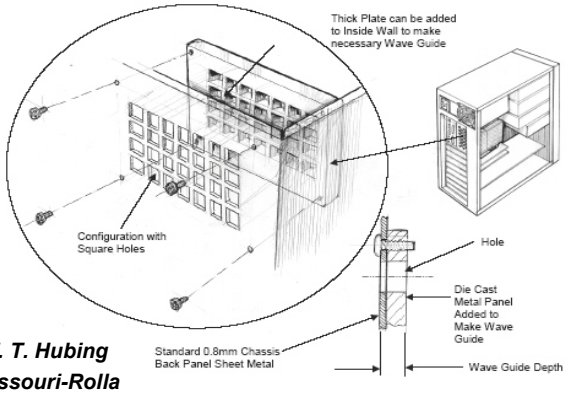
3. How tightly do the lengths of traces in a differential pair need to be controlled to avoid an EMI problem?

- **Match electrical lengths between traces of a pair to minimize skew**
  - Skew between the signals of a pair will result in a phase difference between the signals
  - Destroying magnetic flux cancellation resulting in EMI!
- **The key word is balance!!**



Source: www.LVDS.national.com

2. How large can the apertures in my shielded enclosure be?



Courtesy: Prof. T. Hubing
University of Missouri-Rolla

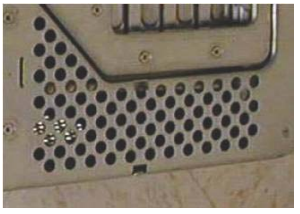
Chapter Colloquium on Electromagnetic Interference (EMI) in Radio Systems: Applications in Communication Engineering, Satellite Communications, Electromagnetic Compatibility, Microwave, antennae and Electron Devices

2. How large can the apertures in my shielded enclosure be?

Correct answer: It depends

- What is the dominant factor determining leakage from the enclosure?

Good answer: Have you looked carefully at your seams?



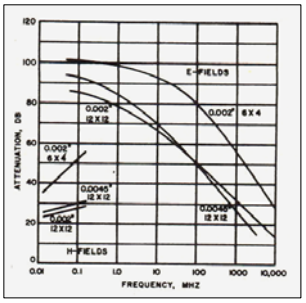
Courtesy: Prof. T. Hubing
University of Missouri-Rolla

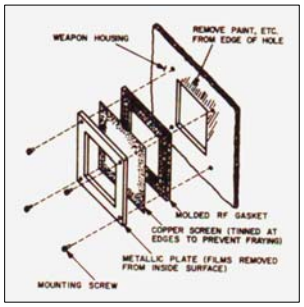
M. Li, J. Drewniak, S. Radu, J. Nuebel, T. Hubing, R. DuBroff and T. Van Doren, "An EMI estimate for shielding-enclosure evaluation," *IEEE Transactions on Electromagnetic Compatibility*, vol. 43, no. 3, Aug. 2001, pp. 295-304.

2. How large can the apertures in my shielded enclosure be?

$$R_a[dB] \approx 20\log\left(\frac{W_{mm}}{\lambda/2}\right)$$

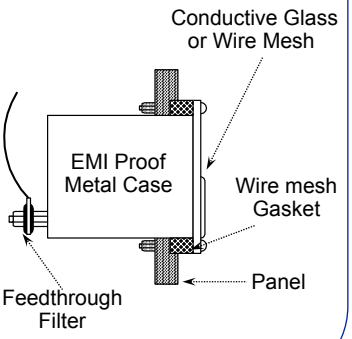
2. How large can the apertures in my shielded enclosure be?





Application of wire mesh shield for displays

Shielding mesh placed in front of the display



1. What are the most important PCB EMC design guidelines?

Correct answer: It depends

Good answer: Design rules won't make you a good circuit board designer:

Use common sense!

1. What are the most important PCB EMC design guidelines?

Just tell me what rules I need to follow to ensure that I don't have EMC-related problems with my printed circuit board design.

Just tell me what rules I need to follow to ensure that I don't have health-related problems with my brain surgery.

Courtesy: Prof. T. Hubing
University of Missouri-Rolla

1. What are the most important PCB EMC design guidelines?

Correct answer: Design rules won't make you a good PCB designer

Good answer:

1. Visualize signal current paths 

2. Locate antennas and crosstalk paths 
3. Be aware of potential EMI sources 

4. Don't let ANY trace or component cross a gap in the ground plane! 
5. Control your transition times 
6. Seek design advice when you need it